In the Claims:

1. (Currently amended) Method of manufacturing a semiconductor device, the method comprising;

providing a semiconductor body of silicon, at a surface thereof, with a first semiconductor region of a first conductivity type, in which region a second semiconductor region of a second conductivity type, opposite to the first conductivity type, is formed forming a pn-junction with the first semiconductor region by the ion implantation of dopant atoms of the second conductivity type into the semiconductor body, and

wherein, before the introduction of said dopant atoms, an amorphous region is formed in the semiconductor body by ~~means of~~ an amorphizing implantation of inert atoms, and wherein, after the amorphizing implantation, temporary dopant atoms are implanted in the semiconductor body before the implantation of the dopant atoms of the second conductivity type, and between these implantations the semiconductor body is low- temperature annealed, and wherein, after introduction of the dopant atoms of the second conductivity type, the semiconductor body is further annealed by subjecting it to a heat treatment at a temperature in the range of about 500 to about 800 degrees Celsius.

2. (Currently amended) Method according to claim 1, characterized in that the semiconductor body is annealed in at least one instance by a heat treatment at a temperature in the range of 550 to about 750 degrees Celsius.

3. (Currently amended) Method according to claim 1, characterized in that the low-temperature anneal implantation of the temporary dopant atom is performed before the implantation of the dopant atoms of the second conductivity type, and between these implantations the semiconductor body is low-temperature annealed by a further heat treatment in the same temperature range as the other heat treatment.

4. (Previously Presented) Method according to claim 1 wherein the semiconductor device is formed as a field effect transistor, in which method the semiconductor body of silicon is provided, at the surface thereof, with a source region and a drain region of the

second conductivity type, which are both provided with extensions, and with a channel region of the first conductivity type between the source region and the drain region, and with a gate region separated from the surface of the semiconductor body by a gate dielectric above the channel region, characterized in that first semiconductor region is formed as a part of the channel region and the source and drain extensions are formed as a part of the second semiconductor region.

5. (Original) Method as claimed in claim 1, characterized in that for the first conductivity type the n-conductivity type is chosen, for the dopant atoms of the second conductivity type Boron atoms are chosen and for the temporary dopant atoms Fluor atoms are chosen.

6. (Previously presented) Method according to claim 3, characterized in that for the amorphizing implantation of inert ions, ions are chosen from a group consisting of Ge, Si, Ar or Xe.

7. (Original) Method as claimed in claim 1, characterized in that for the annealing heat treatments a time is chosen between 1 second and 10 minutes.

8. (Previously Presented) A semiconductor device obtained with a method as claimed in claim 1.

9. (Previously Presented) A semiconductor device as claimed in claim 8, characterized in that the device comprises a field effect transistor.

10. (Currently amended) A method according to claim 1, wherein the further anneal is carried out at a temperature to mitigate the deactivation of the dopant atoms of the second conductivity type.

11. (Currently amended) ~~A method according to claim 1, further including,~~ Method of manufacturing a semiconductor device, the method comprising:

providing a semiconductor body of silicon, at a surface thereof, with a first semiconductor region of a first conductivity type, in which region a second semiconductor region of a second conductivity type, opposite to the first conductivity type, is formed forming a pn-junction with the first semiconductor region by the ion implantation of dopant atoms of the second conductivity type into the semiconductor body, and

wherein, before the introduction of said dopant atoms, an amorphous region is formed in the semiconductor body by an amorphizing implantation of inert atoms, and wherein, after the amorphizing implantation, temporary dopant atoms are implanted in the semiconductor body, and wherein, after introduction of the dopant atoms of the second conductivity type, the semiconductor body is annealed by subjecting it to a heat treatment at a temperature in the range of about 500 to about 800 degrees Celsius,

after introduction of the dopant atoms of the second conductivity type, controlling the temperature of subsequent manufacturing steps for the semiconductor device to not exceed about 800 degrees Celsius.

12. (Previously Presented) A method of manufacturing a semiconductor device having a silicon semiconductor body including a first semiconductor region of a first conductivity type, the method comprising:

implanting inert atoms to form an amorphous region in the first semiconductor region;

after implanting inert atoms,

implanting temporary dopant atoms at the amorphous region,

ion-implanting dopant atoms of a second conductivity type at the amorphous region, the second conductivity type being opposite the first conductivity type; and

after ion-implanting the dopant atoms of a second conductivity type, annealing the semiconductor device via heat treatment at a temperature in the range of about 550 to about 750 degrees Celsius to recover the amorphous region and to form a second semiconductor region including the dopant atoms of the second conductivity type, the first and second semiconductor regions forming a pn-junction therebetween.

13. (Previously Presented) The method of claim 12, wherein the step of annealing includes annealing the semiconductor device at a temperature that mitigates deactivation of the dopant atoms of the second conductivity type.

14. (Previously Presented) The method of claim 12, wherein, after the step of annealing, the temperature of subsequent manufacturing steps for the semiconductor device is controlled to not exceed about 800 degrees Celsius.

15. (Previously Presented) The method of claim 12, wherein the step of implanting temporary dopant atoms is carried out before the step of ion-implanting dopant atoms of a second conductivity type.

16. (Previously Presented) The method of claim 12, wherein the step of implanting temporary dopant atoms is carried out after the step of ion-implanting dopant atoms of a second conductivity type.

17. (Previously Presented) The method of claim 12,

wherein the step of implanting temporary dopant atoms is carried out before the step of ion-implanting dopant atoms of a second conductivity type, and

further including, prior to ion-implanting dopant atoms of a second conductivity type, annealing the semiconductor device via heat treatment at a temperature in the range of about 500 to about 800 degrees Celsius.

18. (Previously Presented) The method of claim 12, wherein the implanting steps are carried out in part of a channel region of a field-effect transistor, adjacent to an active region, to form an extension of the active region that underlies a surface of the channel region.

19. (Previously Presented) The method of claim 12, wherein

the first conductivity type is the n-conductivity type;

ion-implanting dopant atoms of a second conductivity type includes ion-implanting Boron atoms; and

implanting temporary dopant atoms includes implanting Fluor atoms.

20. (Previously Presented) The method of claim 12, wherein implanting inert atoms includes implanting inert atoms selected from the group of: Ge, Si, Ar or Xe.